

AD5625R/AD5645R/AD5665R, AD5625/AD5665

FEATURES

Low power, smallest pin-compatible, quad *nano*DACs

AD5625R/AD5645R/AD5665R

12-/14-/16-bit

On-chip 1.25 V/2.5 V, 5 ppm/°C reference

AD5625/AD5665

12-/16-bit

External reference only

3 mm × 3 mm 10 lead LFCSP and 14-lead TSSOP

2.7 V to 5.5 V power supply

Guaranteed monotonic by design

Power-on reset to zero scale/midscale

Per channel power-down

Hardware LDAC and CLR functions

I²C-compatible serial interface supports standard (100 kHz),
fast (400 kHz), and high speed (3.4 MHz) modes

APPLICATIONS

Process control

Data acquisition systems

Portable battery-powered instruments

Digital gain and offset adjustment

Programmable voltage and current sources

Programmable attenuators

GENERAL DESCRIPTION

The AD5625R/AD5645R/AD5665R and AD5625/AD5665 members of the *nano*DAC family are low power, quad, 12-/14-/16-bit, buffered voltage-out DACs with/without an on-chip reference. All devices operate from a single 2.7 V to 5.5 V supply, are guaranteed monotonic by design, and have an I²C-compatible serial interface.

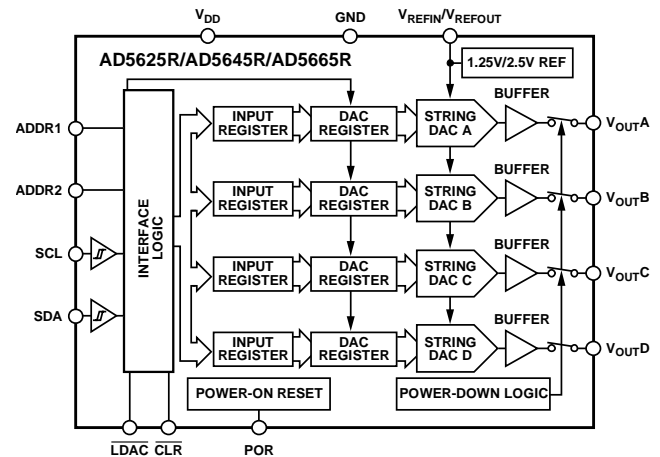
The AD5625R/AD5645R/AD5665R have an on-chip reference. The AD56x5RBCPZ (LFCSP) have a 1.25 V, 5 ppm/°C reference, giving a full-scale output range of 2.5 V; the AD56x5RBRUZ (TSSOP) have a 2.5 V, 5 ppm/°C reference giving a full-scale output range of 5 V. The on-chip reference is off at power-up, allowing the use of an external reference. The internal reference is enabled via a software write. The AD5665/AD5625 require an external reference voltage to set the output range of the DAC.

The part incorporates a power-on reset circuit that ensures the DAC output powers up to 0 V (POR = GND) or midscale (POR = V_{DD}) and remains there until a valid write occurs. The on-chip precision output amplifier enables rail-to-rail output swing.

Rev. 0

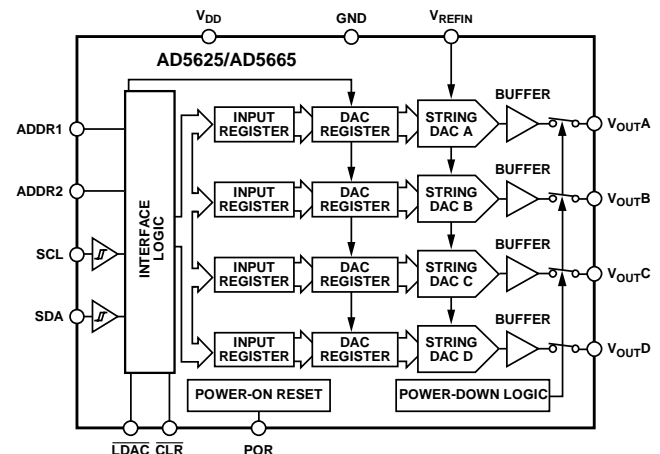
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FUNCTIONAL BLOCK DIAGRAMS



NOTES
1. THE FOLLOWING PINS ARE AVAILABLE ONLY ON 14-LEAD PACKAGE:
ADDR2, LDAC, CLR, POR.

Figure 1. AD5625R/AD5645R/AD5665R



NOTES
1. THE FOLLOWING PINS ARE AVAILABLE ONLY ON 14-LEAD PACKAGE:
ADDR2, LDAC, CLR, POR.

Figure 2. AD5625/AD5665

The AD56x5R/AD56x5 use a 2-wire I²C-compatible serial interface that operates in standard (100 kHz), fast (400 kHz), and high speed (3.4 MHz) modes.

Table 1. Related Devices

Part No.	Description
AD5624R/AD5644R/AD5664R, AD5624/AD5664	Quad SPI 12-/14-/16-bit DACs, with/without internal reference.
AD5627R/AD5647R/AD5667R, AD5627/AD5667	Dual I ² C 12-/14-/16-bit DACs, with/without internal reference.
AD5666	2.7 V to 5.5 V, quad 16-bit DAC, internal reference, SPI interface

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REVISION HISTORY

3/07—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$; $R_L = 2\text{ k}\Omega$ to GND; $C_L = 200\text{ pF}$ to GND; $V_{REFIN} = V_{DD}$; all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Conditions/Comments ¹
STATIC PERFORMANCE²					
AD5665R/AD5665					
Resolution	16			Bits	
Relative Accuracy		±8	±16	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic by design
AD5645R					
Resolution	14			Bits	
Relative Accuracy		±2	±4	LSB	
Differential Nonlinearity			±0.5	LSB	Guaranteed monotonic by design
AD5625R/AD5625					
Resolution	12			Bits	
Relative Accuracy		±0.5	±1	LSB	
Differential Nonlinearity			±0.25	LSB	Guaranteed monotonic by design
Zero-Code Error		2	10	mV	All zeroes loaded to DAC register
Offset Error		±1	±10	mV	
Full-Scale Error		-0.1	±0.5	% of FSR	All ones loaded to DAC register
Gain Error		±0.1	±1	% of FSR	
Zero-Code Error Drift		±2		μV/°C	
Gain Temperature Coefficient		±2.5		ppm	Of FSR/°C
DC Power Supply Rejection Ratio		-100		dB	DAC code = midscale; $V_{DD} = 5\text{ V} \pm 10\%$
DC Crosstalk (External Reference)		15		μV	Due to full-scale output change, $R_L = 2\text{ k}\Omega$ to GND or V_{DD}
		10		μV/mA	Due to load current change
		8		μV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25		μV	Due to full-scale output change, $R_L = 2\text{ k}\Omega$ to GND or V_{DD}
		20		μV/mA	Due to load current change
		10		μV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS³					
Output Voltage Range	0		V_{DD}	V	
Capacitive Load Stability		2		nF	$R_L = \infty$
		10		nF	$R_L = 2\text{ k}\Omega$
DC Output Impedance		0.5		Ω	
Short-Circuit Current		30		mA	$V_{DD} = 5\text{ V}$
Power-Up Time		4		μs	Coming out of power-down mode; $V_{DD} = 5\text{ V}$
REFERENCE INPUTS					
Reference Current		210	260	μA	$V_{REF} = V_{DD} = 5.5\text{ V}$
Reference Input Range	0.75		V_{DD}	V	
Reference Input Impedance		26		kΩ	
REFERENCE OUTPUT (LFCSP)					
Output Voltage	1.247		1.253	V	At ambient
Reference TC ³		±10		ppm/°C	
Output Impedance		7.5		kΩ	
REFERENCE OUTPUT (TSSOP)					
Output Voltage	2.495		2.505	V	At ambient
Reference TC ³		±5	±10	ppm/°C	
Output Impedance		7.5		kΩ	

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Parameter	Min	Typ	Max	Unit	Conditions/Comments ¹
LOGIC INPUTS (ADDRx, CLR, LDAC, POR)³					
I_{IN} , Input Current			± 1	μA	
V_{INL} , Input Low Voltage			$0.15 \times V_{DD}$	V	
V_{INH} , Input High Voltage	$0.85 \times V_{DD}$			V	
C_{IN} , Pin Capacitance		2		pF	
V_{HYST} , Input Hysteresis	$0.1 \times V_{DD}$			V	
LOGIC INPUTS (SDA, SCL)³					
I_{IN} , Input Current			± 1	μA	
V_{INL} , Input Low Voltage			$0.3 \times V_{DD}$	V	
V_{INH} , Input High Voltage	$0.7 \times V_{DD}$			V	
C_{IN} , Pin Capacitance		2		pF	
V_{HYST} , Input Hysteresis	$0.1 \times V_{DD}$			V	High speed mode
	$0.05 \times V_{DD}$			V	Fast mode
LOGIC OUTPUTS (SDA)³					
V_{OL} , Output Low Voltage			0.4	V	$I_{SINK} = 3 \text{ mA}$
			0.6	V	$I_{SINK} = 6 \text{ mA}$
Floating-State Leakage Current			± 1	μA	
Floating-State Output Capacitance		2		pF	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
I_{DD} (Normal Mode) ⁴					$V_{IH} = V_{DD}, V_{IL} = \text{GND}$, full-scale loaded
$V_{DD} = 4.5 \text{ V to } 5.5 \text{ V}$		1.0	1.16	mA	Internal reference off
$V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		0.9	1.05	mA	Internal reference off
$V_{DD} = 4.5 \text{ V to } 5.5 \text{ V}$		1.9	2.14	mA	Internal reference on
$V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$		1.4	1.59	mA	Internal reference on
I_{DD} (All Power-Down Modes) ⁵					
$V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$		0.48	1	μA	$V_{IH} = V_{DD}, V_{IL} = \text{GND}$ (LFCSP)
$V_{DD} = 3.6 \text{ V to } 5.5 \text{ V}$		0.48	1	μA	$V_{IH} = V_{DD}, V_{IL} = \text{GND}$ (TSSOP)

¹ Temperature range of B grade is -40°C to $+105^{\circ}\text{C}$.

² Linearity calculated using a reduced code range: AD5665R (Code 512 to Code 65,024), AD5645R (Code 128 to Code 16,256), AD5625R (Code 32 to Code 4064). Output unloaded.

³ Guaranteed by design and characterization, not production tested.

⁴ Interface inactive. All DACs active. DAC outputs unloaded.

⁵ All DACs powered down. Power-down function is not available on 14-lead TSSOP parts when the part is powered with $V_{DD} < 3.6 \text{ V}$.

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AC CHARACTERISTICS

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$; $R_L = 2\text{ k}\Omega$ to GND; $C_L = 200\text{ pF}$ to GND; $V_{REFIN} = V_{DD}$; all specifications T_{MIN} to T_{MAX} , unless otherwise noted.¹

Table 3.

Parameter ²	Min	Typ	Max	Unit	Conditions/Comments ³
Output Voltage Settling Time					
AD5625R/AD5625		3	4.5	μs	$\frac{1}{4}$ to $\frac{3}{4}$ scale settling to ± 0.5 LSB
AD5645R		3.5	5	μs	$\frac{1}{4}$ to $\frac{3}{4}$ scale settling to ± 0.5 LSB
AD5665R/AD5665		4	7	μs	$\frac{1}{4}$ to $\frac{3}{4}$ scale settling to ± 2 LSB
Slew Rate		1.8		$\text{V}/\mu\text{s}$	
Digital-to-Analog Glitch Impulse					1 LSB change around major carry
		15		$\text{nV}\cdot\text{s}$	LFCSOP
		5		$\text{nV}\cdot\text{s}$	TSSOP
Digital Feedthrough		0.1		$\text{nV}\cdot\text{s}$	
Reference Feedthrough		-90		dB	$V_{REF} = 2\text{ V} \pm 0.1\text{ V p-p}$, frequency 10 Hz to 20 MHz
Digital Crosstalk		0.1		$\text{nV}\cdot\text{s}$	
Analog Crosstalk		1		$\text{nV}\cdot\text{s}$	External reference
		4		$\text{nV}\cdot\text{s}$	Internal reference
DAC-to-DAC Crosstalk		1		$\text{nV}\cdot\text{s}$	External reference
		4		$\text{nV}\cdot\text{s}$	Internal reference
Multiplying Bandwidth		340		kHz	$V_{REF} = 2\text{ V} \pm 0.1\text{ V p-p}$
Total Harmonic Distortion		-80		dB	$V_{REF} = 2\text{ V} \pm 0.1\text{ V p-p}$, frequency = 10 kHz
Output Noise Spectral Density		120		$\text{nV}/\sqrt{\text{Hz}}$	DAC code = midscale, 1 kHz
		100		$\text{nV}/\sqrt{\text{Hz}}$	DAC code = midscale, 10 kHz
Output Noise		15		$\mu\text{V p-p}$	0.1 Hz to 10 Hz

¹ Guaranteed by design and characterization, not production tested.

² See the Terminology section.

³ Temperature range is -40°C to $+105^\circ\text{C}$, typical @ 25°C .

AD5625R/AD5645R/AD5665R, AD5625/AD5665

I²C TIMING SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, f_{SCL} = 3.4 MHz, unless otherwise noted.¹

Table 4.

Parameter	Conditions ²	Min	Max	Unit	Description
f _{SCL} ³	Standard mode		100	kHz	Serial clock frequency
	Fast mode		400	kHz	
	High speed mode, C _B = 100 pF		3.4	MHz	
	High speed mode, C _B = 400 pF		1.7	MHz	
t ₁	Standard mode	4		μs	t _{HIGH} , SCL high time
	Fast mode	0.6		μs	
	High speed mode, C _B = 100 pF	60		ns	
	High speed mode, C _B = 400 pF	120		ns	
t ₂	Standard mode	4.7		μs	t _{LOW} , SCL low time
	Fast mode	1.3		μs	
	High speed mode, C _B = 100 pF	160		ns	
	High speed mode, C _B = 400 pF	320		ns	
t ₃	Standard mode	250		ns	t _{SU;DAT} , data setup time
	Fast mode	100		ns	
	High speed mode	10		ns	
t ₄	Standard mode	0	3.45	μs	t _{HD;DAT} , data hold time
	Fast mode	0	0.9	μs	
	High speed mode, C _B = 100 pF	0	70	ns	
	High speed mode, C _B = 400 pF	0	150	ns	
t ₅	Standard mode	4.7		μs	t _{SU;STA} , setup time for a repeated start condition
	Fast mode	0.6		μs	
	High speed mode	160		ns	
t ₆	Standard mode	4		μs	t _{HD;STA} , hold time (repeated) start condition
	Fast mode	0.6		μs	
	High speed mode	160		ns	
t ₇	Standard mode	4.7		μs	t _{BUF} , bus-free time between a stop and a start condition
	Fast mode	1.3		μs	
t ₈	Standard mode	4		μs	t _{SU;STO} , setup time for a stop condition
	Fast mode	0.6		μs	
	High speed mode	160		ns	
t ₉	Standard mode		1000	ns	t _{RDA} , rise time of SDA signal
	Fast mode		300	ns	
	High speed mode, C _B = 100 pF	10	80	ns	
	High speed mode, C _B = 400 pF	20	160	ns	
t ₁₀	Standard mode		300	ns	t _{FDA} , fall time of SDA signal
	Fast mode		300	ns	
	High speed mode, C _B = 100 pF	10	80	ns	
	High speed mode, C _B = 400 pF	20	160	ns	
t ₁₁	Standard mode		1000	ns	t _{RCL} , rise time of SCL signal
	Fast mode		300	ns	
	High speed mode, C _B = 100 pF	10	40	ns	
	High speed mode, C _B = 400 pF	20	80	ns	
t _{11A}	Standard mode		1000	ns	t _{RCL1} , rise time of SCL signal after a repeated start condition and after an acknowledge bit
	Fast mode		300	ns	
	High speed mode, C _B = 100 pF	10	80	ns	
	High speed mode, C _B = 400 pF	20	160	ns	

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Parameter	Conditions ²	Min	Max	Unit	Description
t ₁₂	Standard mode		300	ns	t _{FCL} , fall time of SCL signal
	Fast mode		300	ns	
	High speed mode, C _B = 100 pF	10	40	ns	
	High speed mode, C _B = 400 pF	20	80	ns	
t ₁₃	Standard mode	10		ns	$\overline{\text{LDAC}}$ pulse width low
	Fast mode	10		ns	
	High speed mode	10		ns	
t ₁₄	Standard mode	300		ns	Falling edge of ninth SCL clock pulse of last byte of a valid write to $\overline{\text{LDAC}}$ falling edge
	Fast mode	300		ns	
	High speed mode	30		ns	
t ₁₅	Standard mode	20		ns	$\overline{\text{CLR}}$ pulse width low
	Fast mode	20		ns	
	High speed mode	20		ns	
t _{SP} ⁴	Fast mode	0	50	ns	Pulse width of spike suppressed
	High speed mode	0	10	ns	

¹ See Figure 3. High speed mode timing specification applies only to the AD5625RBRUZ-2/AD5625RBRUZ-2REEL7 and AD5665RBRUZ-2/AD5665RBRUZ-2REEL7.

² C_B refers to the capacitance on the bus line.

³ The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate but has a negative effect on EMC behavior of the part.

⁴ Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns for fast mode, or less than 10 ns for high speed mode.

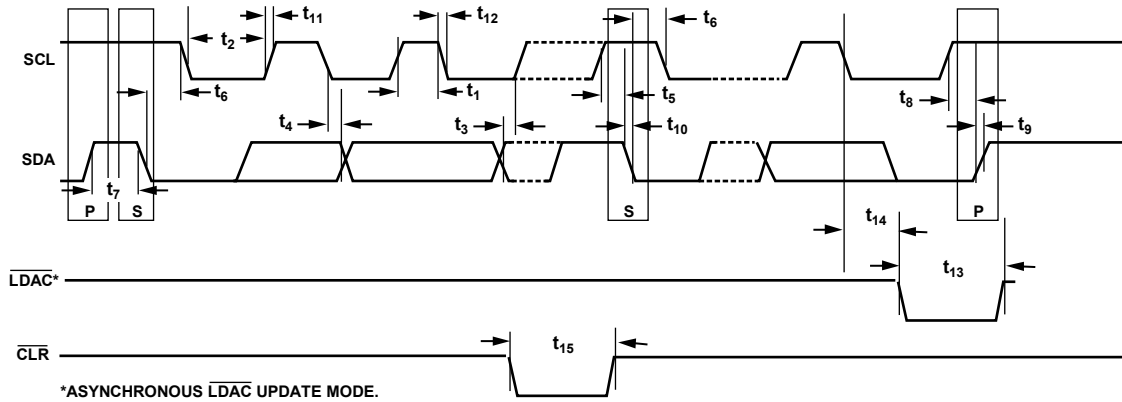


Figure 3. 2-Wire Serial Interface Timing Diagram

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AD5625R/AD5645R/AD5665R, AD5625/AD5665

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V _{DD} to GND	−0.3 V to +7 V
V _{OUT} to GND	−0.3 V to V _{DD} + 0.3 V
V _{REFIN} /V _{REFOUT} to GND	−0.3 V to V _{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V _{DD} + 0.3 V
Operating Temperature Range, Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T _J maximum)	150°C
Power Dissipation	(T _J max − T _A)/θ _{JA}
θ _{JA} Thermal Impedance	
LFCSOP_WD (4-Layer Board)	61°C/W
TSSOP	150.4°C/W
Reflow Soldering Peak Temperature, RoHS Compliant	260°C ± 5°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

AD5625R/AD5645R/AD5665R, AD5625/AD5665

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

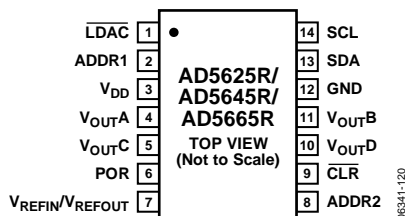


Figure 4. Pin Configuration (14-Lead TSSOP), R Suffix Version

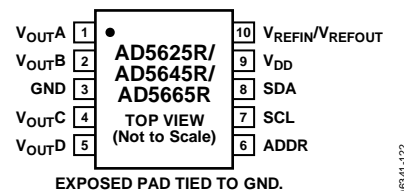


Figure 6. Pin Configuration (10-Lead LFCSP), R Suffix Version

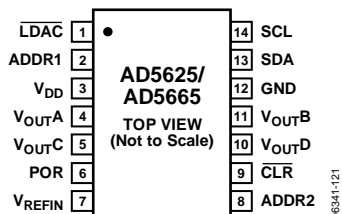


Figure 5. Pin Configuration (14-Lead TSSOP)

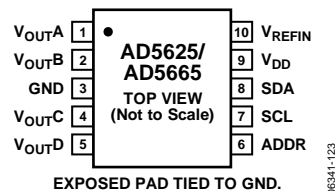


Figure 7. Pin Configuration (10-Lead LFCSP)

Table 6. Pin Function Descriptions

Pin Number		Mnemonic	Description
14-Lead	10-Lead		
1	N/A	LDAC	Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows simultaneous update of all DAC outputs. Alternatively, this pin can be tied permanently low.
2	N/A	ADDR1	Three-State Address Input. Sets the two least significant bits (Bit A1, Bit A0) of the 7-bit slave address (see Table 7).
3	9	V _{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 μF capacitor in parallel with a 0.1 μF capacitor to GND.
4	1	V _{OUTA}	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
5	4	V _{OUTC}	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
6	N/A	POR	Power-On Reset Pin. Tying the POR pin to GND powers up the part to 0 V. Tying the POR pin to V _{DD} powers up the part to midscale.
7	10	V _{REFIN} /V _{REFOUT}	The AD56x5R have a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input. (The internal reference and reference output are only available on R suffix versions.) The AD56x5 has a reference input pin only.
8	N/A	ADDR2	Three-State Address Input. Sets Bit A3 and Bit A2 of the 7-bit slave address (see Table 8).
9	N/A	CLR	Asynchronous Clear Input. The CLR input is falling-edge sensitive. While CLR is low, all LDAC pulses are ignored. When CLR is activated, zero scale is loaded to all input and DAC registers. This clears the output to 0 V. The part exits clear code mode on the falling edge of the ninth clock pulse of the last byte of the valid write. If CLR is activated during a write sequence, the write is aborted. If CLR is activated during high speed mode, the part exits high speed mode.
10	5	V _{OUTD}	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
11	2	V _{OUTB}	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
12	3	GND	Ground reference point for all circuitry on the part.
13	8	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into or out of the 16-bit input register. It is a bidirectional, open-drain data line that should be pulled to the supply with an external pull-up resistor.
14	7	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into or out of the 16-bit input register.
N/A	6	ADDR	Three-State Address Input. Sets the two least significant bits (Bit A1, Bit A0) of the 7-bit slave address (see Table 7).

TYPICAL PERFORMANCE CHARACTERISTICS

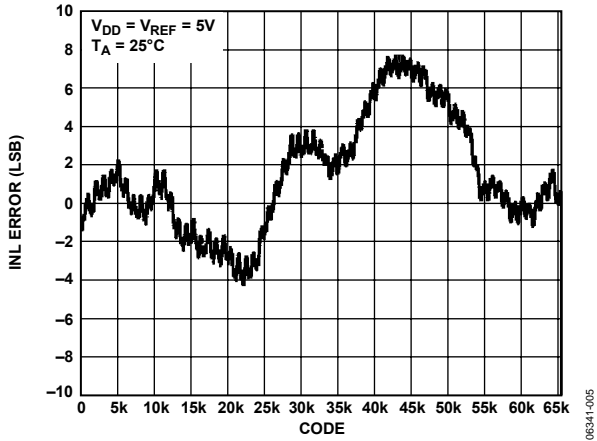


Figure 8. INL AD5665, External Reference

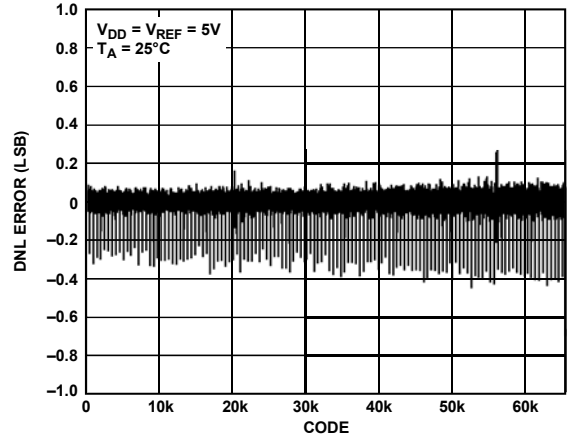


Figure 11. DNL AD5665, External Reference

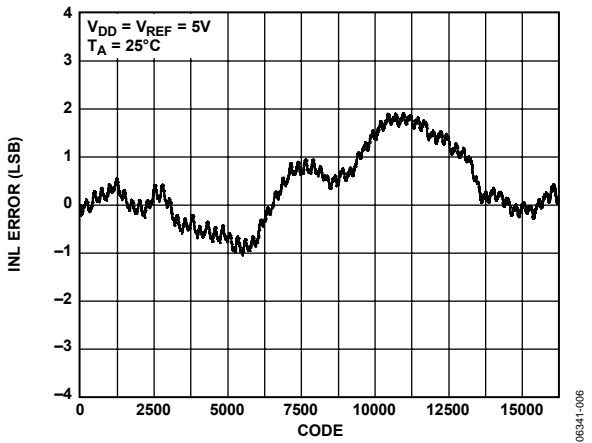


Figure 9. INL AD5645R, External Reference

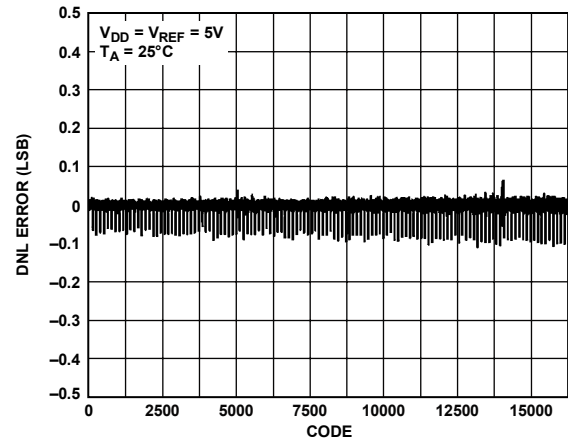


Figure 12. DNL AD5645R, External Reference

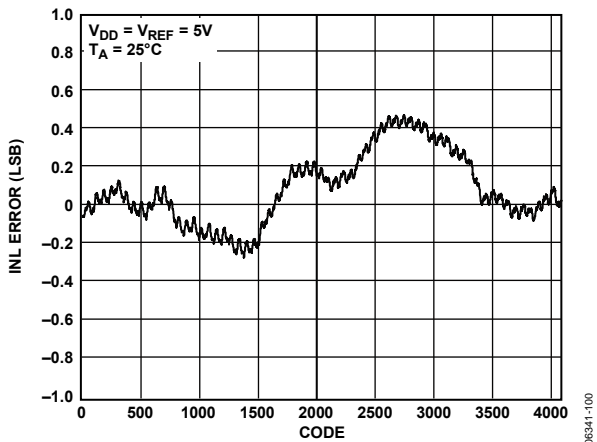


Figure 10. INL AD5625, External Reference

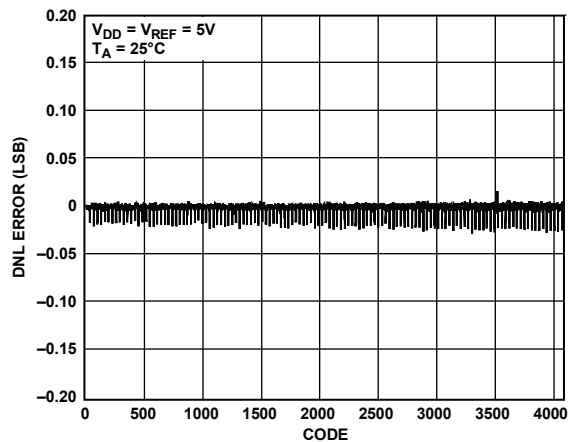


Figure 13. DNL AD5625, External Reference

AD5625R/AD5645R/AD5665R, AD5625/AD5665

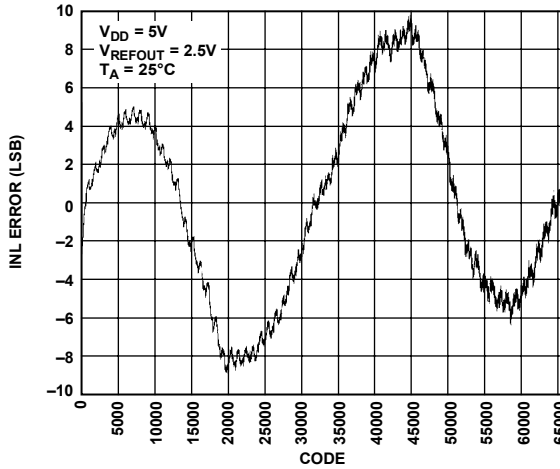


Figure 14. INL AD5665R, 2.5 V Internal Reference

06341-010

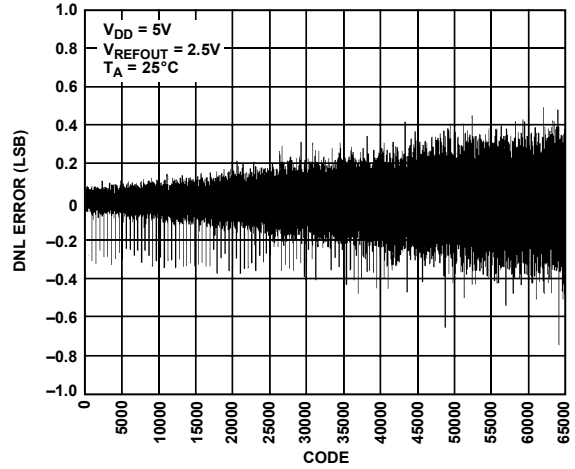


Figure 17. DNL AD5665R, 2.5 V Internal Reference

06341-013

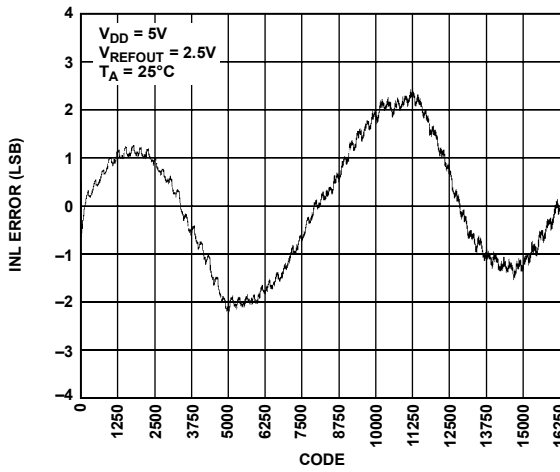


Figure 15. INL AD5645R, 2.5 V Internal Reference

06341-011

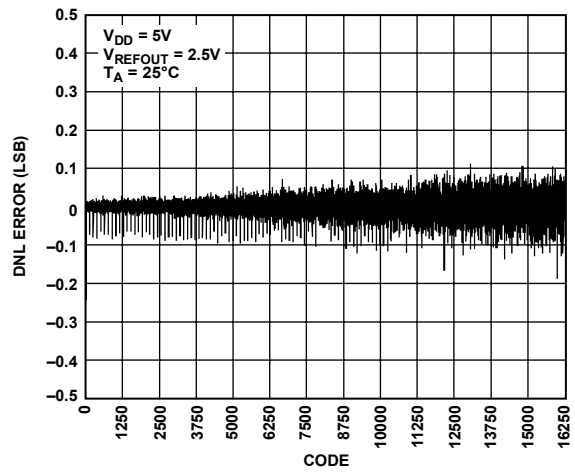


Figure 18. DNL AD5645R, 2.5 V Internal Reference

06341-014

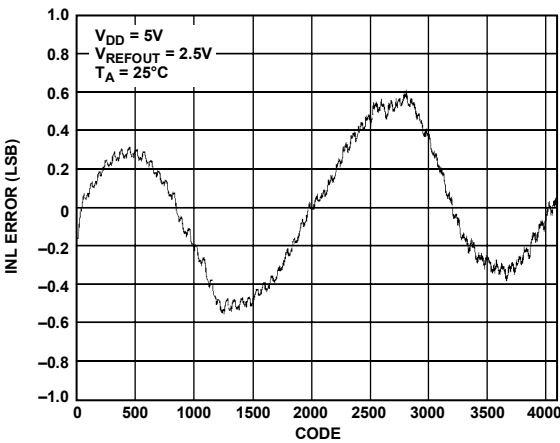


Figure 16. INL AD5625R, 2.5 V Internal Reference

06341-012

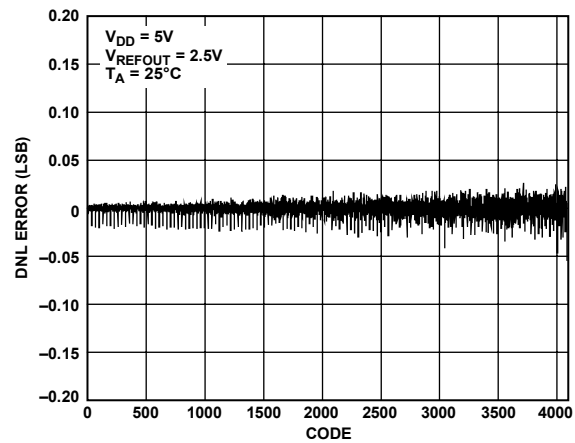


Figure 19. DNL AD5625R, 2.5 V Internal Reference

06341-015

AD5625R/AD5645R/AD5665R, AD5625/AD5665

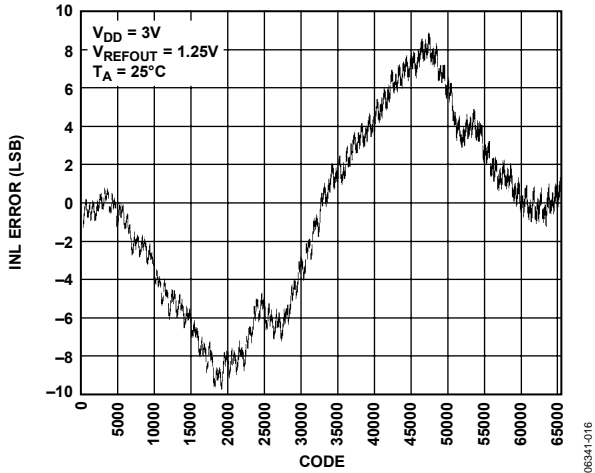


Figure 20. INL AD5665R, 1.25 V Internal Reference

06341-016

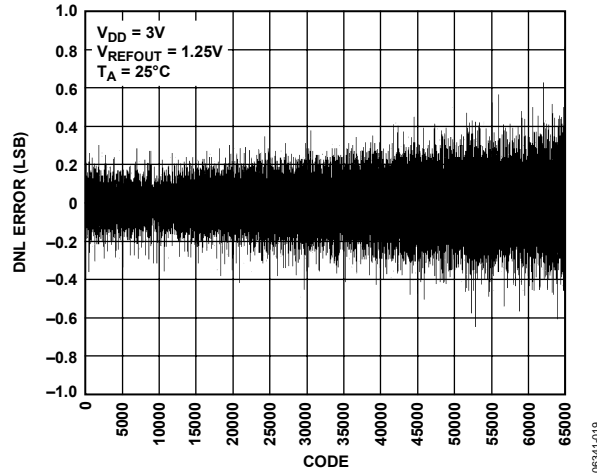


Figure 23. DNL AD5665R, 1.25 V Internal Reference

06341-019

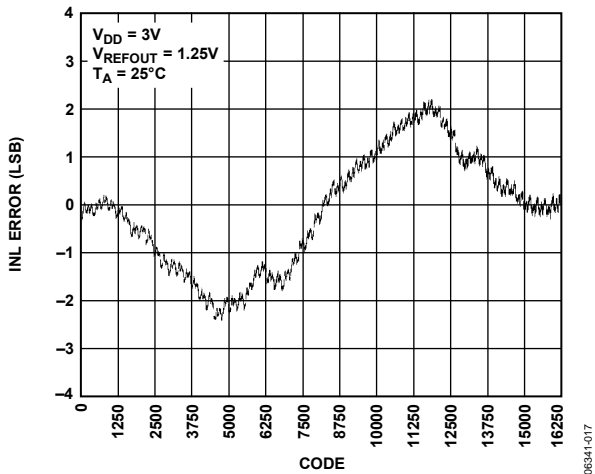


Figure 21. INL AD5645R, 1.25 V Internal Reference

06341-017

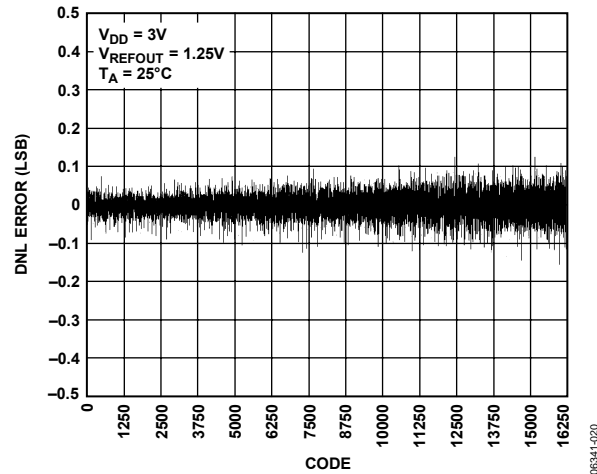


Figure 24. DNL AD5645R, 1.25 V Internal Reference

06341-020

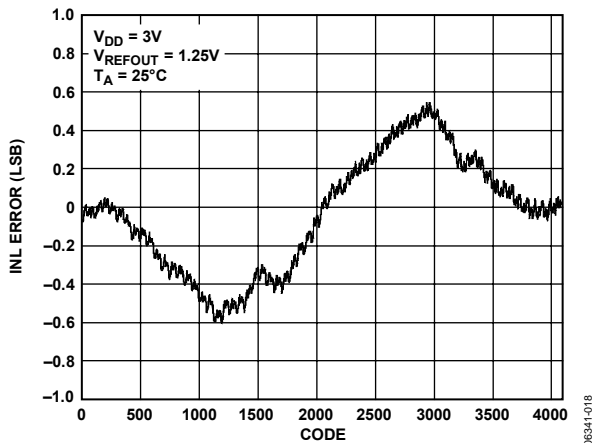


Figure 22. INL AD5625R, 1.25 V Internal Reference

06341-018

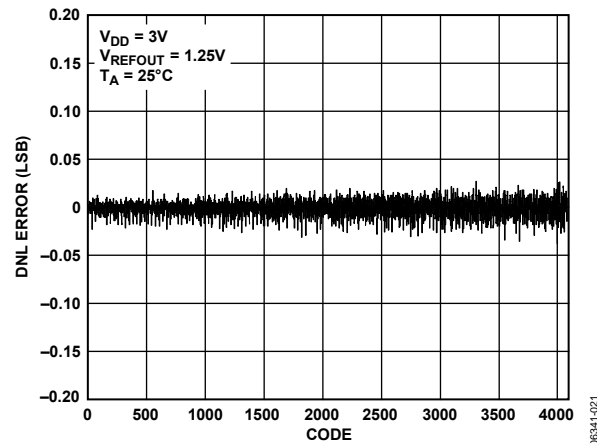


Figure 25. DNL AD5625R, 1.25 V Internal Reference

06341-021

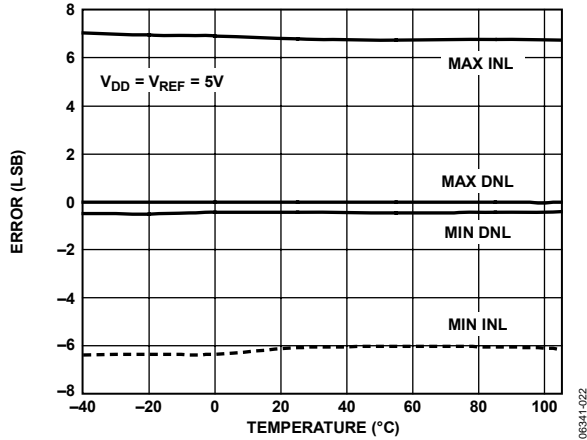


Figure 26. INL Error and DNL Error vs. Temperature

06341-022

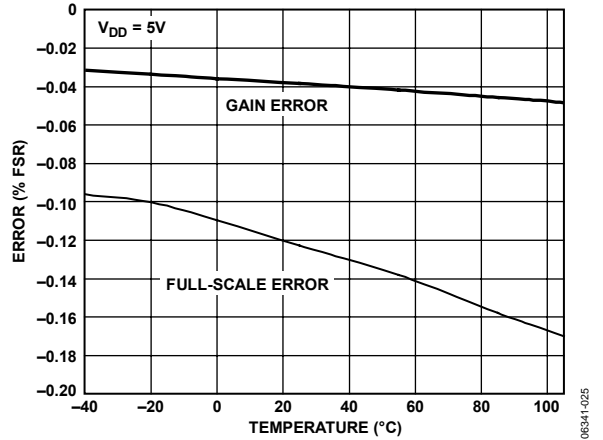


Figure 29. Gain Error and Full-Scale Error vs. Temperature

06341-025

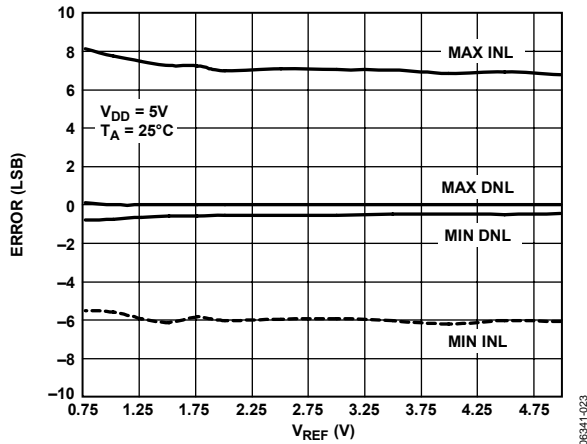


Figure 27. INL and DNL Error vs. V_{REF}

06341-023

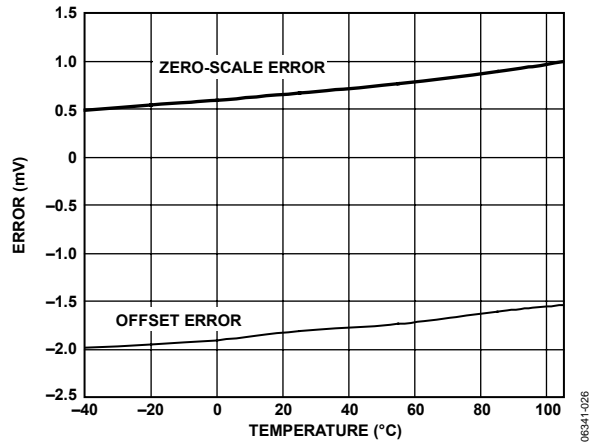


Figure 30. Zero-Scale Error and Offset Error vs. Temperature

06341-026

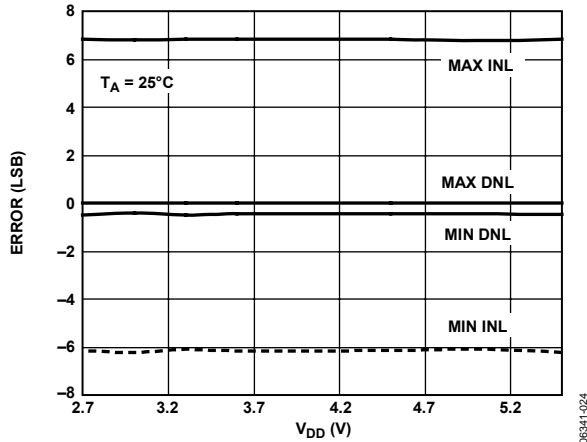


Figure 28. INL and DNL Error vs. Supply

06341-024

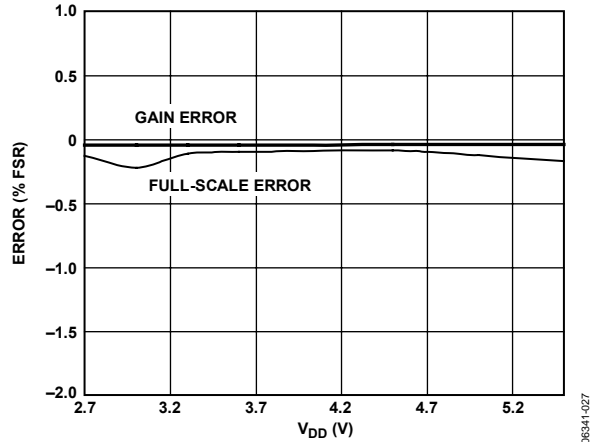


Figure 31. Gain Error and Full-Scale Error vs. Supply

06341-027

AD5625R/AD5645R/AD5665R, AD5625/AD5665

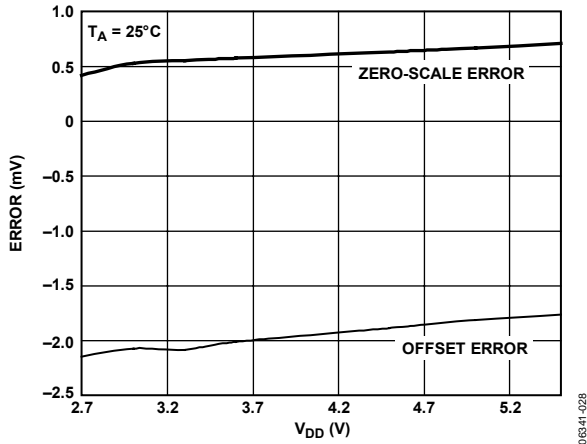


Figure 32. Zero-Scale Error and Offset Error vs. Supply

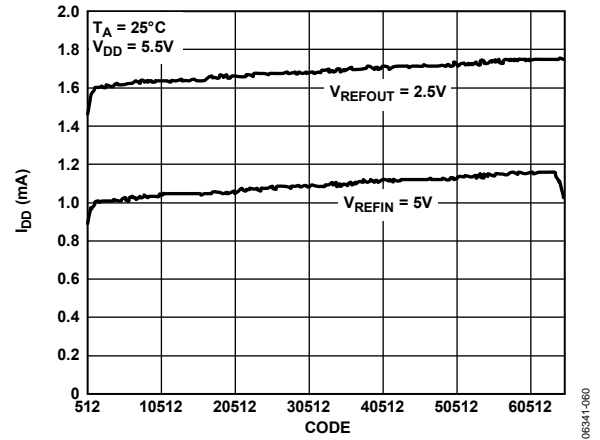


Figure 35. Supply Current vs. DAC Code

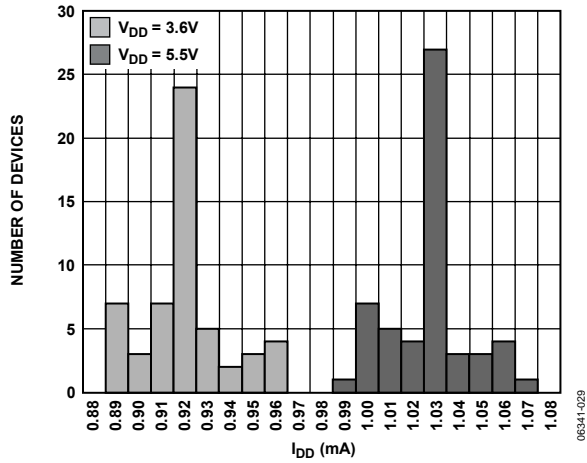


Figure 33. I_{DD} Histogram with External Reference

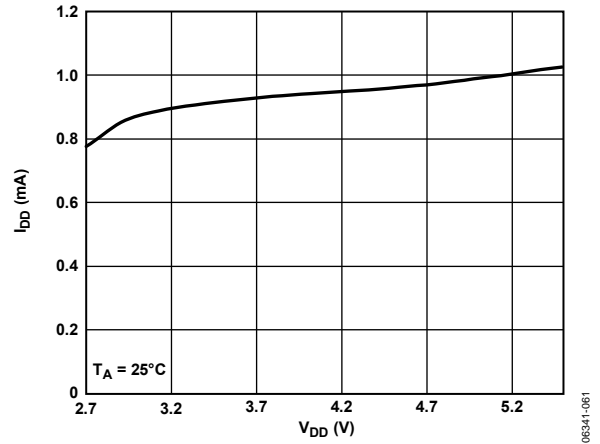


Figure 36. Supply Current vs. Supply

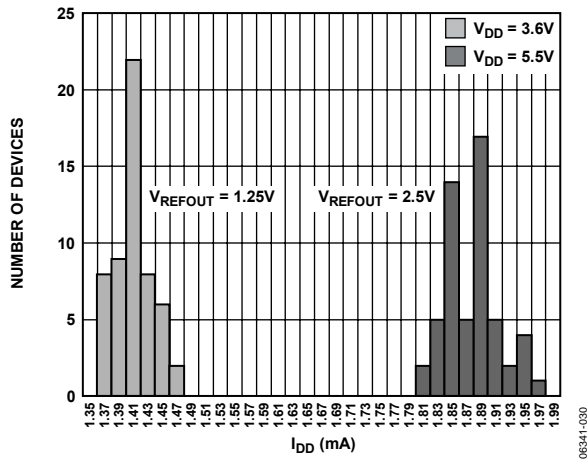


Figure 34. I_{DD} Histogram with Internal Reference

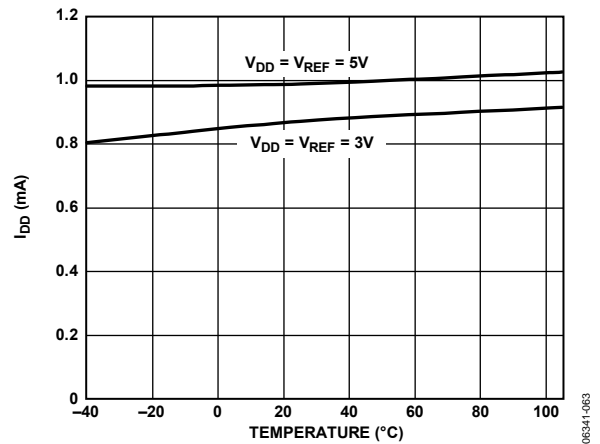


Figure 37. Supply Current vs. Temperature

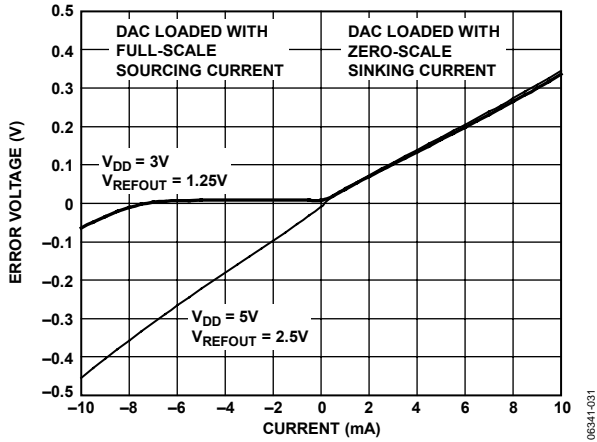


Figure 38. Headroom at Rails vs. Source and Sink

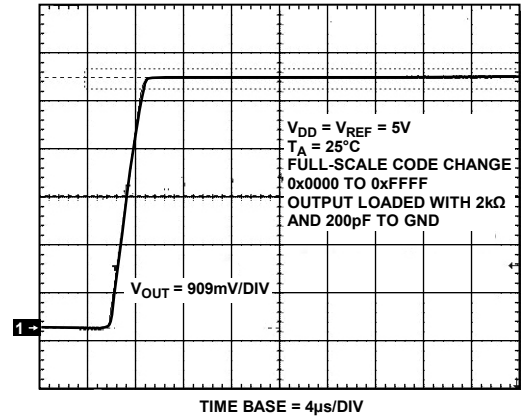


Figure 41. Full-Scale Settling Time, 5 V

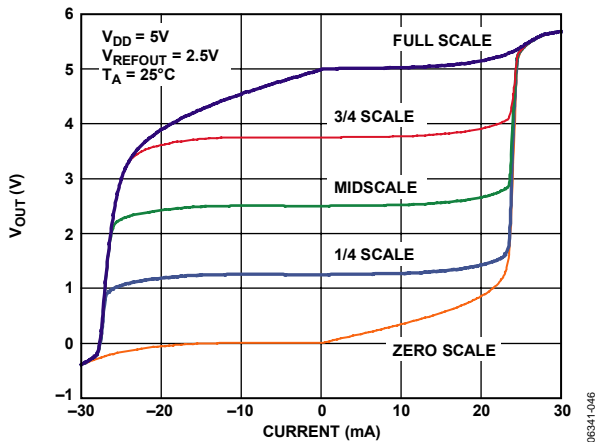


Figure 39. AD56x5R with 2.5 V Reference, Source and Sink Capability

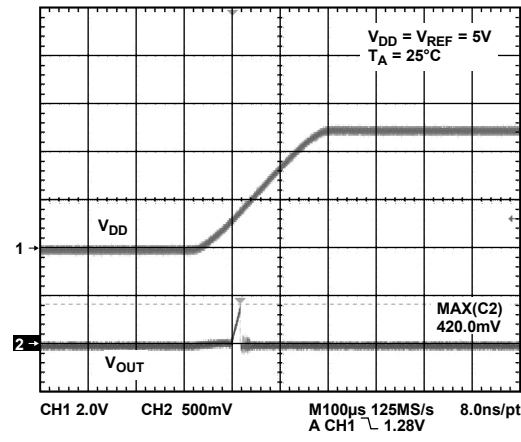


Figure 42. Power-On Reset to 0 V

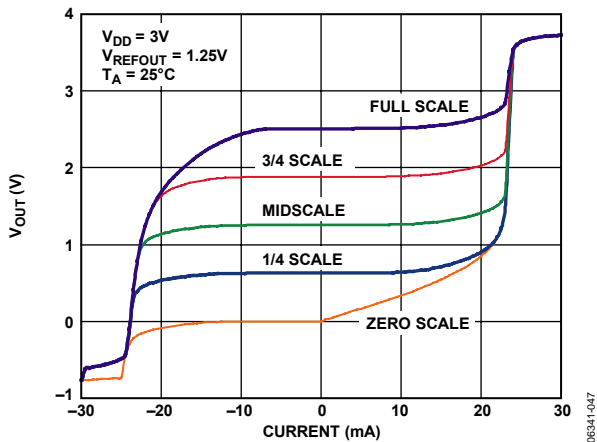


Figure 40. AD56x5R with 1.25 V Reference, Source and Sink Capability

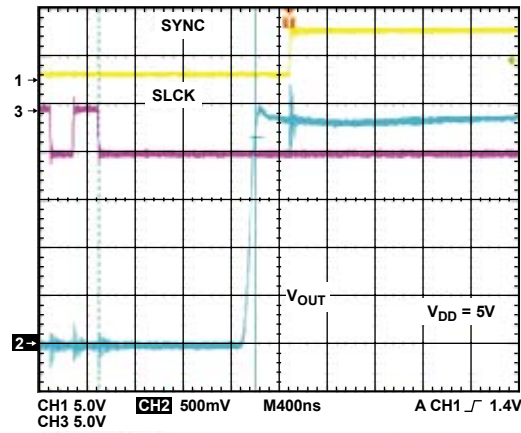


Figure 43. Exiting Power-Down to Midscale

AD5625R/AD5645R/AD5665R, AD5625/AD5665

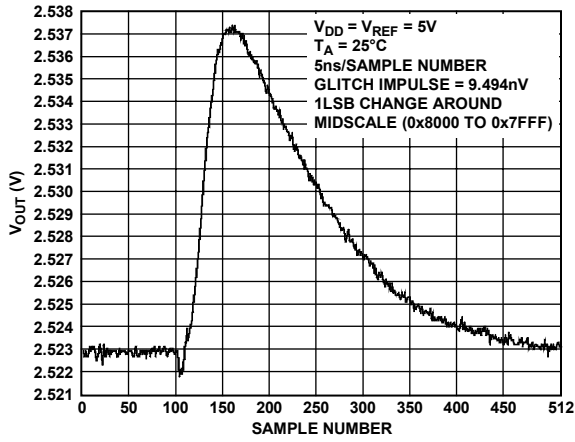


Figure 44. Digital-to-Analog Glitch Impulse (Negative)

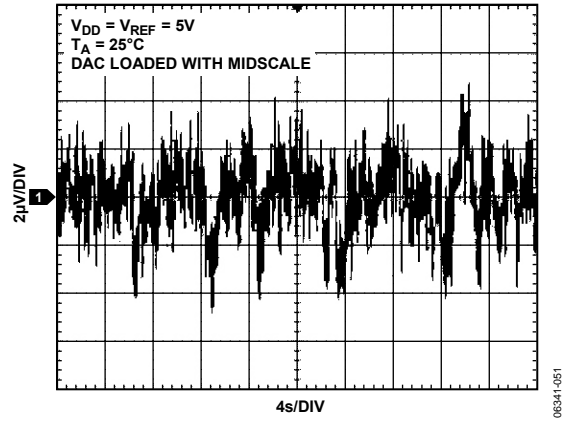


Figure 47. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

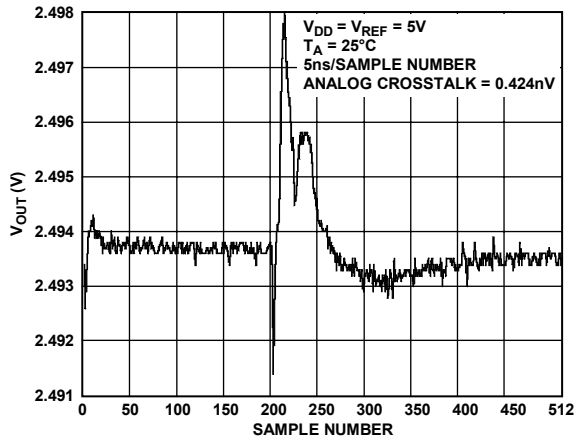


Figure 45. Analog Crosstalk, External Reference

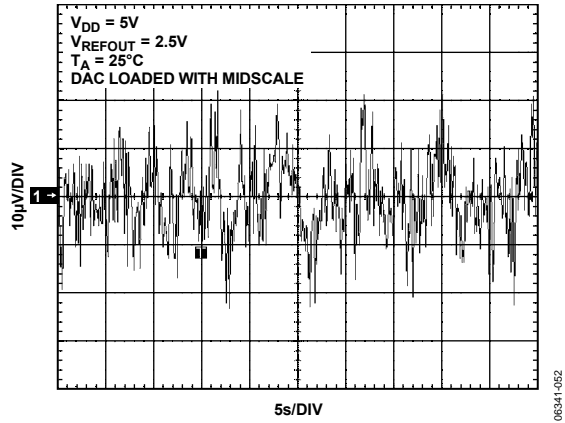


Figure 48. 0.1 Hz to 10 Hz Output Noise Plot, 2.5 V Internal Reference

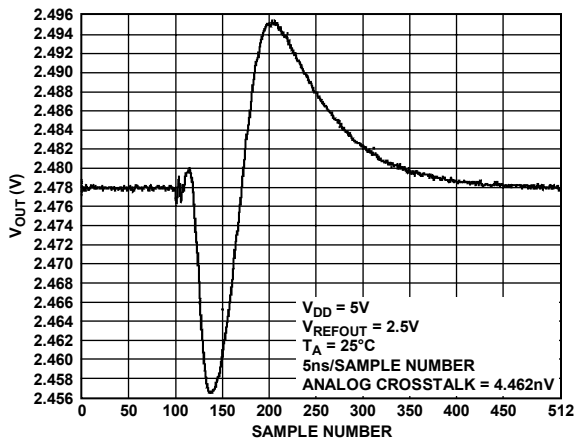


Figure 46. Analog Crosstalk, Internal Reference

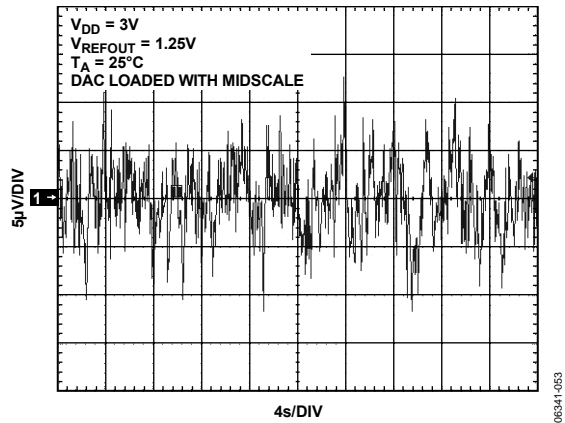


Figure 49. 0.1 Hz to 10 Hz Output Noise Plot, 1.25 V Internal Reference

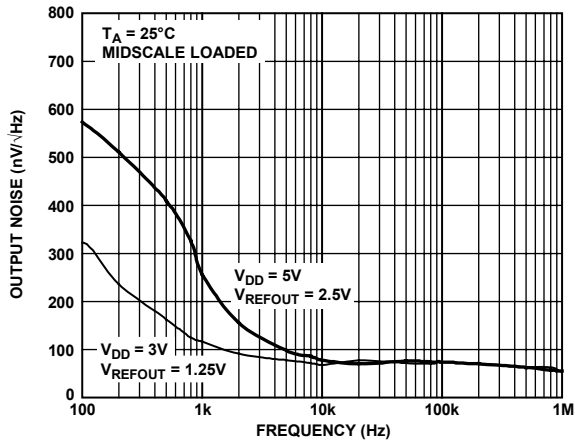


Figure 50. Noise Spectral Density, Internal Reference

06341-054

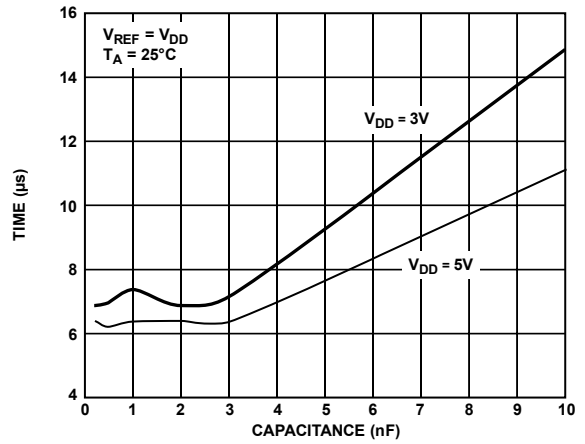


Figure 52. Settling Time vs. Capacitive Load

06341-056

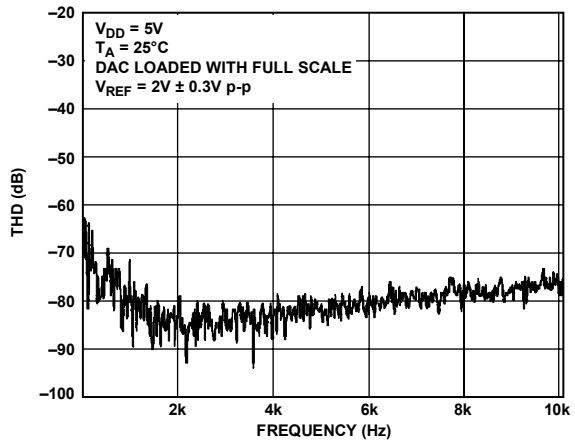


Figure 51. Total Harmonic Distortion

06341-055

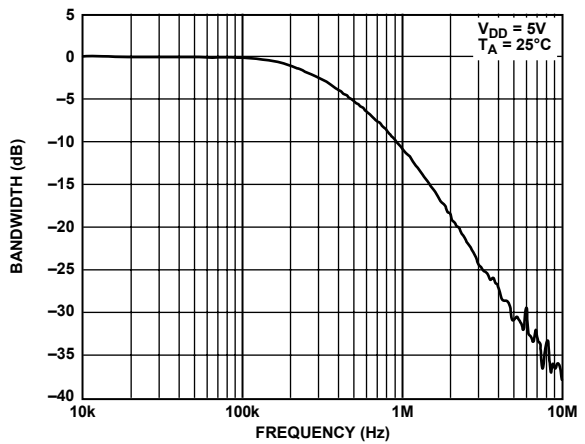


Figure 53. Multiplying Bandwidth

06341-057

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design.

Zero-Code Error

Zero-code error is a measurement of the output error when zero scale (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5665R because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero-code error is expressed in mV.

Full-Scale Error

Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be $V_{DD} - 1$ LSB. Full-scale error is expressed as a percentage of full-scale range (FSR).

Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percentage of FSR.

Zero-Code Error Drift

Zero-code error drift is a measurement of the change in zero-code error with a change in temperature. It is expressed in $\mu\text{V}/^\circ\text{C}$.

Gain Temperature Coefficient

Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/ $^\circ\text{C}$.

Offset Error

Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the AD5665R with Code 512 loaded in the DAC register. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)

DC PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to the change in V_{DD} for full-scale output of the DAC. It is measured in dB. V_{REF} is held at 2 V, and V_{DD} is varied by $\pm 10\%$.

Output Voltage Settling Time

Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a $\frac{1}{4}$ to $\frac{3}{4}$ full-scale input change, and it is measured from the rising edge of the stop condition.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000) (see Figure 44).

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s and is measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Reference Feedthrough

Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. It is expressed in dB.

Output Noise Spectral Density

Output noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density ($\text{nV}/\sqrt{\text{Hz}}$). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in $\text{nV}/\sqrt{\text{Hz}}$. A plot of noise spectral density is shown in Figure 50.

DC Crosstalk

DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in μV .

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has on another DAC kept at midscale. It is expressed in $\mu\text{V}/\text{mA}$.

Digital Crosstalk

This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-s.

Analog Crosstalk

Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) and then executing a software LDAC and monitoring the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa) with $\overline{\text{LDAC}}$ low while monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth

The multiplying bandwidth is a measure of the finite bandwidth of the amplifiers within the DAC. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)

THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

THEORY OF OPERATION

D/A SECTION

The AD56x5R/AD56x5 DACs are fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Figure 54 shows a block diagram of the DAC architecture.

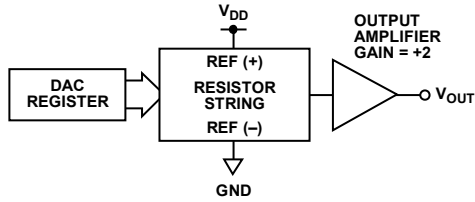


Figure 54. DAC Architecture

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REFIN} \times \left(\frac{D}{2^N} \right)$$

The ideal output voltage when using the internal reference is given by

$$V_{OUT} = 2 \times V_{REFOUT} \times \left(\frac{D}{2^N} \right)$$

where:

D is the decimal equivalent of the binary code that is loaded to the DAC register:

- 0 to 4095 for AD5625R/AD5625 (12-bit).
- 0 to 16,383 for AD5645R (14-bit).
- 0 to 65,535 for AD5665R/AD5665 (16-bit).

N is the DAC resolution.

RESISTOR STRING

The resistor string is shown in Figure 55. It is simply a string of resistors, each of value R . The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

OUTPUT AMPLIFIER

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD} . It can drive a load of 2 k Ω in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier are shown in Figure 38 and Figure 39. The slew rate is 1.8 V/ μ s with a $\frac{1}{4}$ to $\frac{3}{4}$ full-scale settling time of 7 μ s.

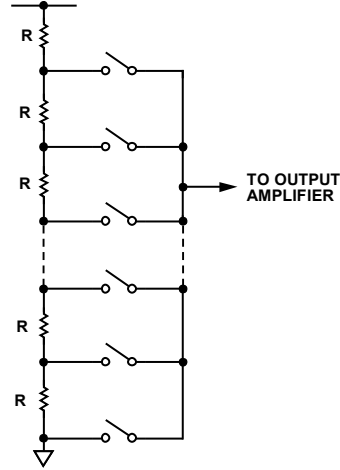


Figure 55. Resistor String

INTERNAL REFERENCE

The AD5625R/AD5645R/AD5665R feature an on-chip reference. Versions without the R suffix require an external reference. The on-chip reference is off at power-up and is enabled via a write to a control register. See the Internal Reference Setup section for details.

Versions packaged in a 10-lead LFCSP have a 1.25 V reference, giving a full-scale output of 2.5 V. These parts can be operated with a V_{DD} supply of 2.7 V to 5.5 V. Versions packaged in a 14-lead TSSOP have a 2.5 V reference, giving a full-scale output of 5 V. Parts are functional with a V_{DD} supply of 2.7 V to 5.5 V, but with a V_{DD} supply of less than 5 V, the output is clamped to V_{DD} . See the Ordering Guide for a full list of models. The internal reference associated with each part is available at the V_{REFOUT} pin (only available on R suffix versions).

A buffer is required if the reference output is used to drive external loads. When using the internal reference, it is recommended that a 100 nF capacitor is placed between the reference output and GND for reference stability.

EXTERNAL REFERENCE

The V_{REFIN} pin on the AD56x5R allows the use of an external reference if the application requires it. The default condition of the on-chip reference is off at power-up. All devices can be operated from a single 2.7 V to 5.5 V supply.

SERIAL INTERFACE

The AD56x5R/AD56x5 have 2-wire I²C-compatible serial interfaces (refer to *The I²C-Bus Specification*, Version 2.1, January 2000, available from Philips Semiconductor). The AD56x5R/AD56x5 can be connected to an I²C bus as a slave device, under the control of a master device. See Figure 3 for a timing diagram of a typical write sequence.

The AD56x5R/AD56x5 support standard (100 kHz), fast (400 kHz), and high speed (3.4 MHz) data transfer modes. High speed operation is only available on selected models. See the Ordering Guide for a full list of models. Support is not provided for 10-bit addressing and general call addressing.

The AD56x5R/AD56x5 each has a 7-bit slave address. The 10-lead versions of the part have a slave address whose five MSBs are 00011, and the two LSBs are set by the state of the ADDR address pin, which determines the state of the A0 and A1 address bits. The 14-lead versions of the part have a slave address whose three MSBs are 001, and the four LSBs are set by the ADDR1 and ADDR2 address pins, which determine the state of the A0 and A1, A2 and A3 address bits, respectively.

The facility to make hardwired changes to the ADDR pin allows the user to incorporate up to three of these devices on one bus, as outlined in Table 7.

Table 7. ADDR Pin Settings (10-Lead Package)

ADDR Pin Connection	A1	A0
V _{DD}	0	0
NC	1	0
GND	1	1

The facility to make hardwired changes to the ADDR1 and the ADDR2 pins allows the user to incorporate up to nine of these devices on one bus, as outlined in Table 8.

Table 8. ADDR1, ADDR2 Pin Settings (14-Pin Package)

ADDR2 Pin Connection	ADDR1 Pin Connection	A3	A2	A1	A0
V _{DD}	V _{DD}	0	0	0	0
V _{DD}	NC	0	0	1	0
V _{DD}	GND	0	0	1	1
NC	V _{DD}	1	0	0	0
NC	NC	1	0	1	0
NC	GND	1	0	1	1
GND	V _{DD}	1	1	0	0
GND	NC	1	1	1	0
GND	GND	1	1	1	1

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address. The slave address corresponding to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its shift register.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits have been read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master brings the SDA line low before the 10th clock pulse, and then high during the 10th clock pulse to establish a stop condition.

WRITE OPERATION

When writing to the AD56x5R/AD56x5, the user must begin with a start command followed by an address byte ($R/\overline{W} = 0$), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The AD5665 requires two bytes of data for the DAC and a command byte that controls various DAC functions. Three bytes of data must therefore be written to the DAC, the command byte followed by the most significant data byte and the least significant data byte, as shown in Figure 56 and Figure 57. After these data bytes are acknowledged by the AD56x5R/AD56x5, a stop condition follows.

READ OPERATION

When reading data back from the AD56x5R/AD56x5, the user begins with a start command followed by an address byte ($R/\overline{W} = 1$), after which the DAC acknowledges that it is prepared to transmit data by pulling SDA low. Two bytes of data are then read from the DAC, which are both acknowledged by the master as shown in Figure 58 and Figure 59. A stop condition follows.

AD5625R/AD5645R/AD5665R, AD5625/AD5665

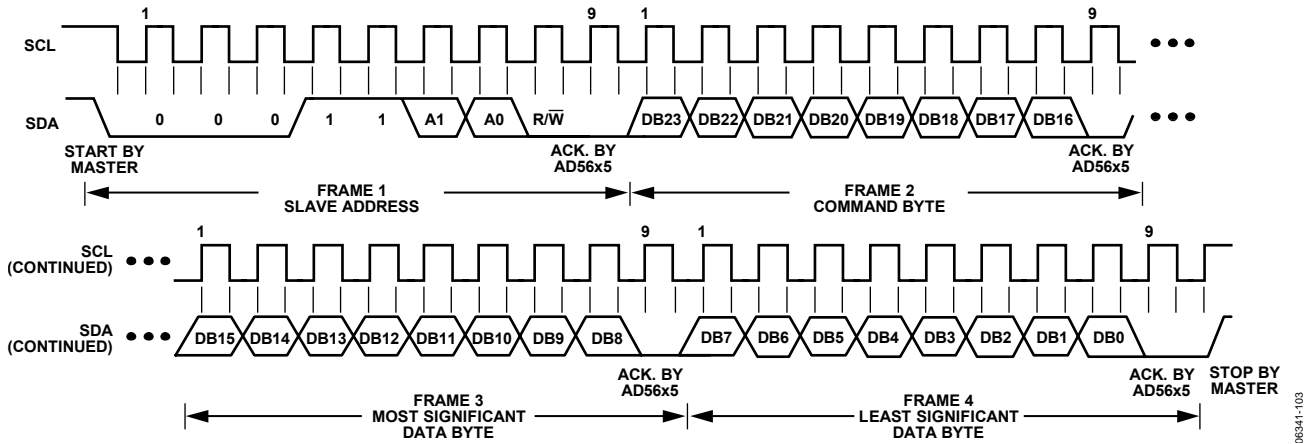


Figure 56. I²C Write Operation (10-Lead Package)

06341-103

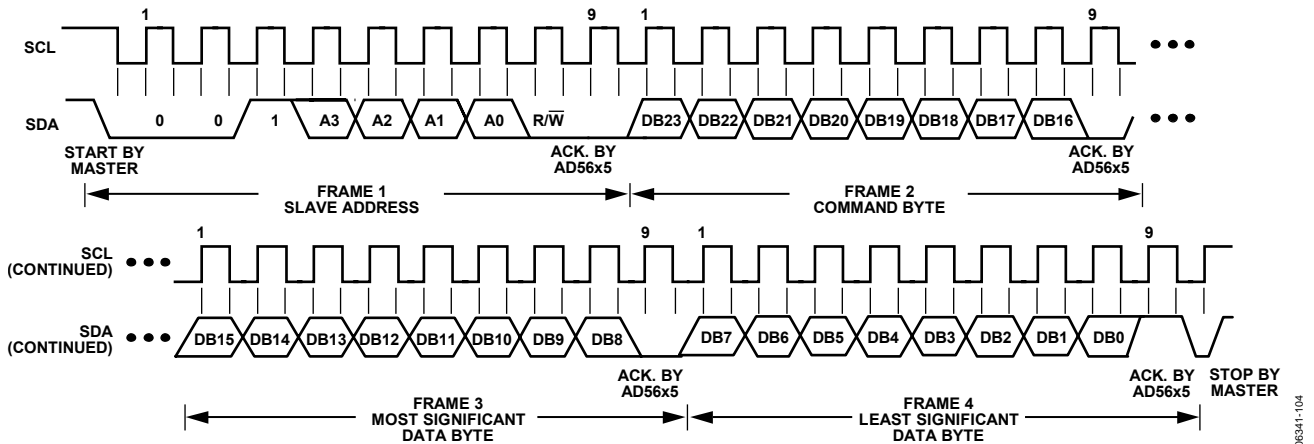


Figure 57. I²C Write Operation (14-Lead Package)

06341-104

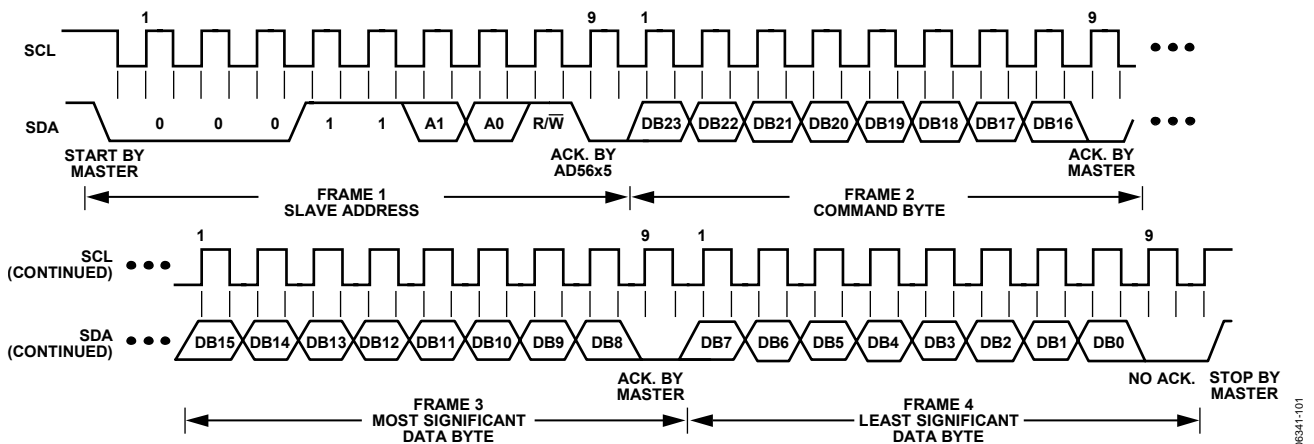
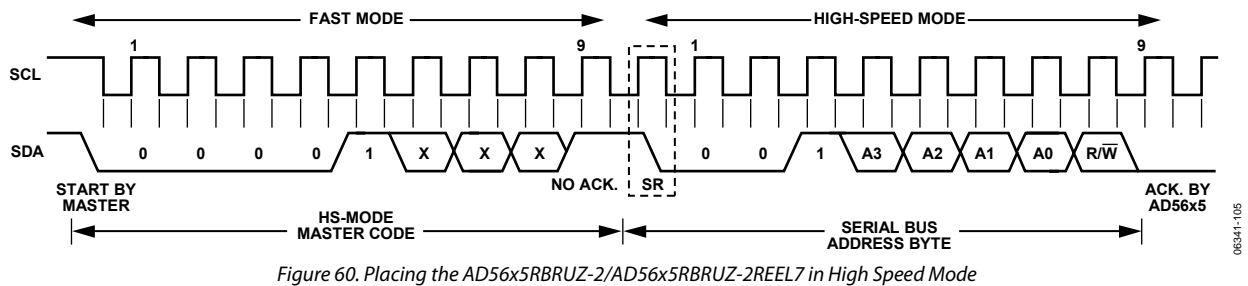
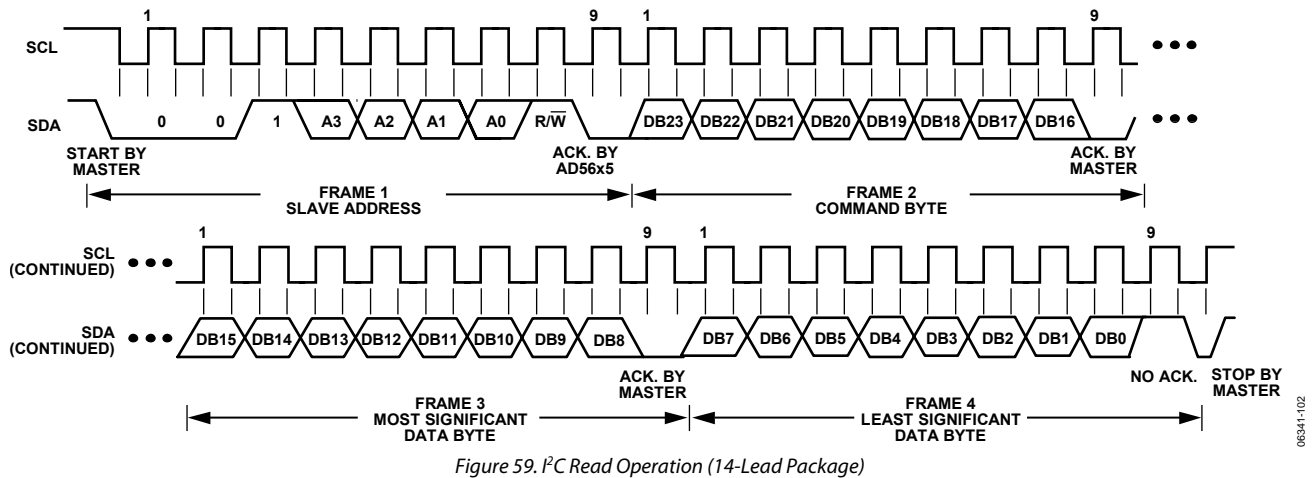


Figure 58. I²C Read Operation (10-Lead Package)

06341-101



HIGH SPEED MODE

Some models offer high speed serial communication with a clock frequency of 3.4 MHz. See the Ordering Guide for a full list of models.

High speed mode communication commences after the master addresses all devices connected to the bus with the Master Code 00001XXX to indicate that a high speed mode transfer is to begin. No device connected to the bus is permitted to acknowledge the high speed master code; therefore, the code is followed by a no acknowledge. Next, the master must issue a repeated start followed by the device address. The selected device then acknowledges its address. All devices continue to operate in high speed mode until the master issues a stop condition. When the stop condition is issued, the devices return to standard/fast mode. The part also returns to standard/fast mode when CLR is activated while the part is in high speed mode.

INPUT SHIFT REGISTER

The input shift register is 24 bits wide. Data is loaded into the device as a 24-bit word under the control of a serial clock input, SCL. The timing diagram for this operation is shown in Figure 3. The eight MSBs make up the command byte. DB23 is reserved and should always be set to 0 when writing to the device. DB22 (S) is used to select multiple byte operation. The next three bits are the command bits (C2, C1, and C0) that control the mode of operation of the device. See Table 9 for details. The last three bits of the first byte are the address bits (A2, A1, and A0). See Table 10 for details. The rest of the bits are the 16-/14-/12-bit data word. The data word comprises the 16-/14-/12-bit input code followed by two or four don't cares for the AD5645R and the AD5625R/AD5625, respectively (see Figure 63 through Figure 65).

MULTIPLE BYTE OPERATION

Multiple byte operation is supported on the AD56x5R/AD56x5. A 2-byte operation is useful for applications that require fast DAC updating and do not need to change the command byte. The S bit (DB22) in the command register can be set to 1 for 2-byte mode of operation (see Figure 62). For standard 3-byte and 4-byte operation, the S bit (DB22) in the command byte should be set to 0 (see Figure 61).

AD5625R/AD5645R/AD5665R, AD5625/AD5665

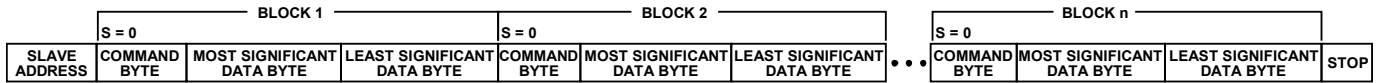


Figure 61. Multiple Block Write with Command Byte in Each Block (S = 0)

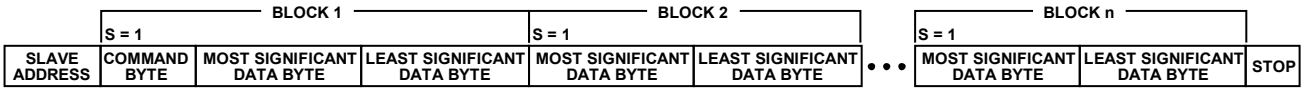


Figure 62. Multiple Block Write with Initial Command Byte Only (S = 1)

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	S	C2	C1	C0	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RESERVED	BYTE SELECTION	COMMAND			DAC ADDRESS			DAC DATA								DAC DATA							
		COMMAND BYTE			DATA HIGH BYTE								DATA LOW BYTE										

Figure 63. AD5665R/AD5665 Input Shift Register (16-Bit DAC)

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	S	C2	C1	C0	A2	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X
RESERVED	BYTE SELECTION	COMMAND			DAC ADDRESS			DAC DATA								DAC DATA							
		COMMAND BYTE			DATA HIGH BYTE								DATA LOW BYTE										

Figure 64. AD5645R Input Shift Register (14-Bit DAC)

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	S	C2	C1	C0	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
RESERVED	BYTE SELECTION	COMMAND			DAC ADDRESS			DAC DATA								DAC DATA							
		COMMAND BYTE			DATA HIGH BYTE								DATA LOW BYTE										

Figure 65. AD5625R/AD5625 Input Shift Register (12-Bit DAC)

BROADCAST MODE

Broadcast addressing is supported on the AD56x5R/AD56x5 only in write mode. Broadcast addressing can be used to synchronously update or power down multiple AD56x5R/AD56x5 devices. Using the broadcast address, the AD56x5R/AD56x5 responds regardless of the states of the address pins. The AD56x5R/AD56x5 broadcast address is 00010000.

Table 9. Command Definition

C2	C1	C0	Command
0	0	0	Write to input Register n
0	0	1	Update DAC Register n
0	1	0	Write to input Register n, update all (software LDAC)
0	1	1	Write to and update DAC Channel n
1	0	0	Power up/power down
1	0	1	Reset
1	1	0	LDAC register setup
1	1	1	Internal reference setup (on/off)

Table 10. DAC Address Command

A2	A1	A0	ADDRESS (n)
0	0	0	DAC A
0	0	1	DAC B
0	1	0	DAC C
0	1	1	DAC D
1	1	1	All DACs

LDAC FUNCTION

The AD56x5R/AD56x5 DACs have double-buffered interfaces consisting of two banks of registers: input registers and DAC registers. The input registers are connected directly to the input shift register, and the digital code is transferred to the relevant input register upon completion of a valid write sequence. The DAC registers contain the digital code used by the resistor strings.

Access to the DAC registers is controlled by the $\overline{\text{LDAC}}$ pin. When the $\overline{\text{LDAC}}$ pin is high, the DAC registers are latched and the input registers can change state without affecting the contents of the DAC registers. When $\overline{\text{LDAC}}$ is brought low, however, the DAC registers become transparent and the contents of the input registers are transferred to them. The double-buffered interface is useful if the user requires simultaneous updating of all DAC outputs. The user can write to one of the input registers individually and then, by bringing $\overline{\text{LDAC}}$ low when writing to the other DAC input register, all outputs update simultaneously.

These parts each contain an extra feature whereby a DAC register is not updated unless its input register has been updated since the last time $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the input registers. In the case of the AD56x5R/AD56x5, the DAC register updates only if the input register has changed since the last time the DAC register was updated, thereby removing unnecessary digital crosstalk.

The outputs of all DACs can be simultaneously updated, using the hardware $\overline{\text{LDAC}}$ pin.

AD5625R/AD5645R/AD5665R, AD5625/AD5665

Synchronous $\overline{\text{LDAC}}$

The DAC registers are updated after new data is read in. $\overline{\text{LDAC}}$ can be permanently low or pulsed.

Asynchronous $\overline{\text{LDAC}}$

The outputs are not updated at the same time that the input registers are written to. When $\overline{\text{LDAC}}$ goes low, the DAC registers are updated with the contents of the input register.

The $\overline{\text{LDAC}}$ register gives the user full flexibility and control over the hardware $\overline{\text{LDAC}}$ pin (and software $\overline{\text{LDAC}}$ on the 10-lead parts that do not have the hardware $\overline{\text{LDAC}}$ pin—see Table 11). This register allows the user to select which combination of channels to simultaneously update when the hardware $\overline{\text{LDAC}}$ pin is executed. Setting the $\overline{\text{LDAC}}$ bit register to 0 for a DAC channel means that the update of this channel is controlled by the $\overline{\text{LDAC}}$ pin. If this bit is set to 1, this channel synchronously updates, that is, the DAC register is updated after new data is read in, regardless of the state of the $\overline{\text{LDAC}}$ pin. The device effectively sees the $\overline{\text{LDAC}}$ pin as being pulled low. See Table 12 for the $\overline{\text{LDAC}}$ register mode of operation. This flexibility is useful in applications when the user wants to simultaneously update select channels while the rest of the channels are synchronously updating.

Writing to the DAC using Command 110 loads the 4-bit $\overline{\text{LDAC}}$ register [DB3:DB0]. The default for each channel is 0, that is, the $\overline{\text{LDAC}}$ pin works normally. Setting the bits to 1 means the DAC register is updated, regardless of the state of the $\overline{\text{LDAC}}$ pin. See Figure 66 for the contents of the input shift register during the $\overline{\text{LDAC}}$ register setup command.

Table 11. $\overline{\text{LDAC}}$ Register Mode of Operation on 10-Lead LFCSP (Load DAC Register)

$\overline{\text{LDAC}}$ Bits (DB3 to DB0)	$\overline{\text{LDAC}}$ Mode of Operation
0	Normal operation (default), DAC register update is controlled by write command.
1	The DAC registers are updated after new data is read in.

Table 12. $\overline{\text{LDAC}}$ Register Mode of Operation on 14-Lead TSSOP (Load DAC Register)

$\overline{\text{LDAC}}$ Bits (DB3 to DB0)	$\overline{\text{LDAC}}$ Pin	$\overline{\text{LDAC}}$ Operation
0	1/0	Determined by $\overline{\text{LDAC}}$ pin.
1	x = don't care	The DAC registers are updated after new data is read in.

R	S	C2	C1	C0	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	X	1	1	0	A2	A1	A0	X	X	X	X	X	X	X	X	X	X	X	X	DAC D	DAC C	DAC B	DAC A
RESERVED	DON'T CARE	COMMAND			DAC ADDRESS (DON'T CARE)			DON'T CARE								DON'T CARE				DAC SELECT (0 = $\overline{\text{LDAC}}$ PIN ENABLED)			

Figure 66. $\overline{\text{LDAC}}$ Setup Command

08341-115

POWER-DOWN MODES

Command 100 is reserved for the power-up/power-down function. The power-up/power-down modes are programmed by setting Bit DB5 and Bit DB4. This defines the output state of the DAC amplifier, as shown in Table 13. Bit DB3 to Bit DB0 determine to which DAC or DACs the power-up/power-down command is applied. Setting one of these bits to 1 applies the power-up/power-down state defined by DB5 and DB4 to the corresponding DAC. If a bit is 0, the state of the DAC is unchanged. Figure 68 shows the contents of the input shift register for the power-up/power-down command.

When Bit DB5 and Bit DB4 are set to 0, the part works normally with its normal power consumption of 1 mA at 5 V. However, for the three power-down modes, the supply current falls to 480 nA at 5 V. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This allows the output impedance of the part to be known while the part is in power-down mode. The outputs can either be connected internally to GND through a 1 kΩ or 100 kΩ resistor, or be left open-circuited (three-state) as shown in Figure 66.

Note that the 14-lead TSSOP models offer the power-down function when the part is operated with a V_{DD} of 3.6 V to 5.5 V. The 10-lead LFCSP models offer the power-down function when the part is powered with a V_{DD} of 2.7 V to 5.5 V.

Table 13. Modes of Operation for the AD56x5R/AD56x5

DB5	DB4	Operating Mode
0	0	Normal operation
		Power-down modes
0	1	1 kΩ pull-down resistor to GND
1	0	100 kΩ pull-down resistor to GND
1	1	Three-state, high impedance

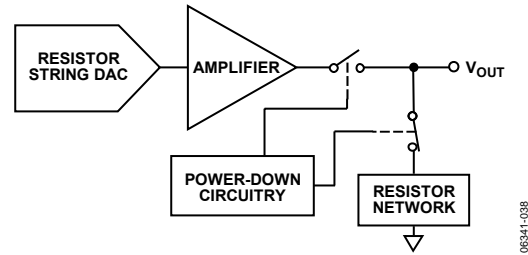


Figure 67. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry are shut down when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 4 μs for $V_{DD} = 5\text{ V}$ or $V_{DD} = 3\text{ V}$.

R	S	C2	C1	C0	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	X	1	0	0	A2	A1	A0	X	X	X	X	X	X	X	X	X	X	PD1	PD0	DAC D	DAC C	DAC B	DAC A
RESERVED	DON'T CARE	COMMAND			DAC ADDRESS (DON'T CARE)			DON'T CARE								DON'T CARE	POWER-DOWN MODE	DAC SELECT (1 = DAC SELECTED)					

Figure 68. Power-Up/Power-Down Command

AD5625R/AD5645R/AD5665R, AD5625/AD5665

POWER-ON RESET AND SOFTWARE RESET

The AD56x5R/AD56x5 contain a power-on reset circuit that controls the output voltage during power-up. The 10-lead version of the device powers up to 0 V. The 14-lead version has a power-on reset (POR) pin that allows the output voltage to be selected. By connecting the POR pin to GND, the AD56x5R/AD56x5 output powers up to 0 V; by connecting the POR pin to V_{DD}, the AD56x5R/AD56x5 output powers up to midscale. The output remains powered up at this level until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

Any events on $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$ during power-on reset are ignored.

There is also a software reset function. Command 101 is the software reset command. The software reset command contains two reset modes that are software programmable by setting bit DB0 in the input shift register.

Table 14 shows how the state of the bit corresponds to the software reset modes of operation of the devices. Figure 69 shows the contents of the input shift register during the software reset mode of operation.

Table 14. Software Reset Modes for the AD56x5R/AD56x5

DB0	Registers Reset to Zero
0	DAC register Input shift register
1 (Power-On Reset)	DAC register Input shift register $\overline{\text{LDAC}}$ register Power-down register Internal reference setup register

INTERNAL REFERENCE SETUP (R VERSIONS)

The on-chip reference is off at power-up by default. It can be turned on by sending the reference setup command (111) and setting DB0 in the input shift register. Table 15 shows how the state of the bit corresponds to the mode of operation.

Table 15. Reference Setup Command

DB0	Action
0	Internal reference off (default)
1	Internal reference on

X	S	C2	C1	C0	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	X	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	RST
RESERVED	DON'T CARE	COMMAND			DAC ADDRESS (DON'T CARE)			DON'T CARE								DON'T CARE					RESET MODE			

Figure 69. Reset Command

R	S	C2	C1	C0	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	X	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	REF
RESERVED	DON'T CARE	COMMAND			DAC ADDRESS (DON'T CARE)			DON'T CARE								DON'T CARE					REFERENCE MODE			

Figure 70. Reference Setup Command

APPLICATION INFORMATION

USING A REFERENCE AS A POWER SUPPLY FOR THE AD56x5R/AD56x5

Because the supply current required by the AD56x5R/AD56x5 is extremely low, an alternative option is to use a voltage reference to supply the required voltage to the part (see Figure 71). This is especially useful if the power supply is noisy, or if the system supply voltages are at some value other than 5 V or 3 V, for example, 15 V. The voltage reference outputs a steady supply voltage for the AD56x5R/AD56x5. If the low dropout REF195 is used, it must supply 450 μ A of current to the AD56x5R/AD56x5 with no load on the output of the DAC. When the DAC output is loaded, the REF195 also needs to supply the current to the load. The total current required (with a 5 k Ω load on the DAC output) is

$$1 \text{ mA} + (5 \text{ V}/5 \text{ k}\Omega) = 2 \text{ mA}$$

The load regulation of the REF195 is typically 2 ppm/mA, resulting in a 4 ppm (20 μ V) error for the 2 mA current drawn from it. This corresponds to a 0.263 LSB error.

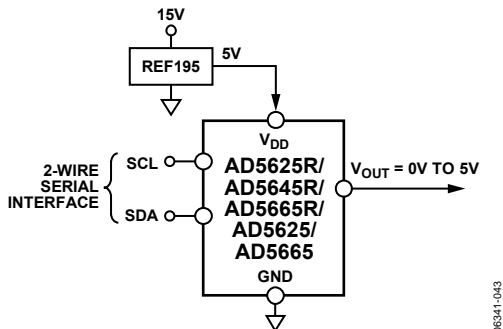


Figure 71. REF195 as Power Supply to the AD56x5R/AD56x5

BIPOLAR OPERATION USING THE AD56x5R/AD56x5

The AD56x5R/AD56x5 have been designed for single-supply operation, but a bipolar output range is also possible using the circuit shown in Figure 72. The circuit gives an output voltage range of ± 5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{DD} \times \left(\frac{D}{65,536} \right) \times \left(\frac{R1 + R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0 to 65,535).

If $V_{DD} = 5$ V, $R1 = R2 = 10$ k Ω ,

$$V_O = \left(\frac{10 \times D}{65,536} \right) - 5 \text{ V}$$

This is an output voltage range of ± 5 V, with 0x0000 corresponding to a -5 V output and 0xFFFF corresponding to a $+5$ V output.

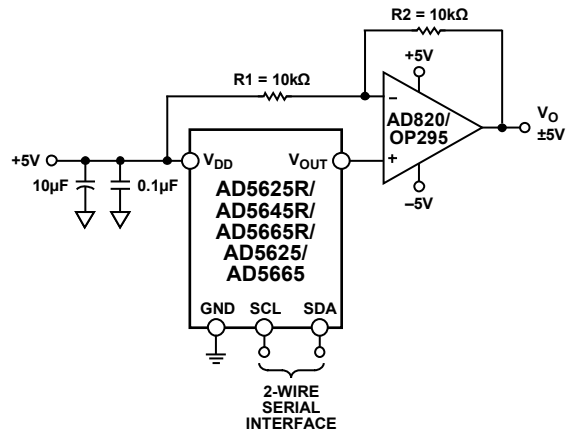


Figure 72. Bipolar Operation with the AD56x5R/AD56x5

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD56x5R/AD56x5 should have separate analog and digital sections, each having its own area of the board. If the AD56x5R/AD56x5 are in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD56x5R/AD56x5.

The power supply to the AD56x5R/AD56x5 should be bypassed with 10 μ F and 0.1 μ F capacitors. The capacitors should be located as close as possible to the device, with the 0.1 μ F capacitor ideally right up against the device. The 10 μ F capacitor is the tantalum bead type. It is important that the 0.1 μ F capacitor have low effective series resistance (ESR) and low effective series inductance (ESI), for example, common ceramic types of capacitors. This 0.1 μ F capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and to reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

AD5625R/AD5645R/AD5665R, AD5625/AD5665

OUTLINE DIMENSIONS

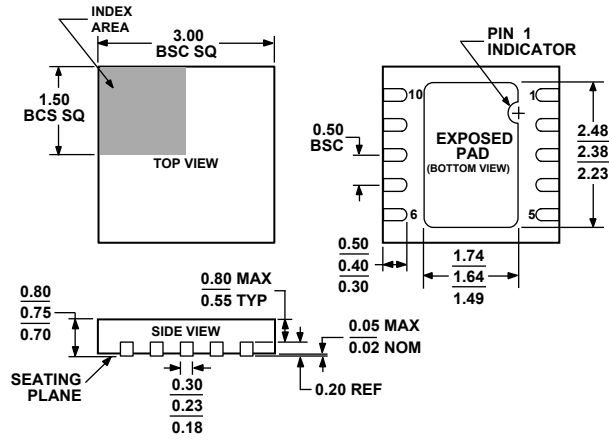
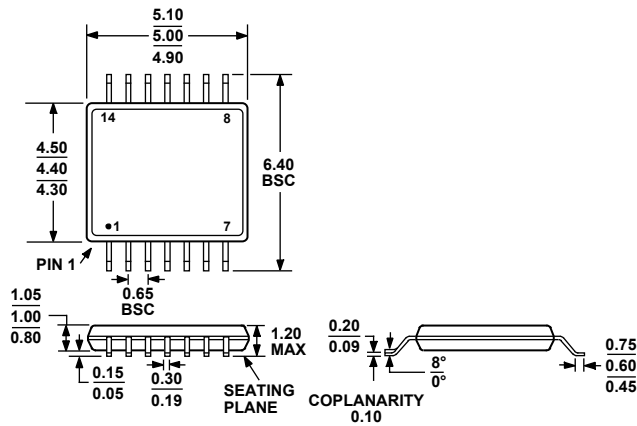


Figure 69. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
 3 mm x 3 mm Body, Very Very Thin, Dual Lead
 (CP-10-9)
 Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1
 Figure 70. 14-Lead Thin Shrink Small Outline Package [TSSOP]
 (RU-14)
 Dimensions shown in millimeters

AD5625R/AD5645R/AD5665R, AD5625/AD5665

ORDERING GUIDE

Model	Temperature Range	Accuracy	On-Chip Reference	Maximum I ² C Speed	Package Description	Package Option	Branding
AD5625BCPZ-R2 ¹	-40°C to +105°C	±1 LSB INL	None	400 kHz	10-Lead LFCSP_WD	CP-10 -9	D8V
AD5625BCPZ-REEL7 ¹	-40°C to +105°C	±1 LSB INL	None	400 kHz	10-Lead LFCSP_WD	CP-10-9	D8V
AD5625BRUZ ¹	-40°C to +105°C	±1 LSB INL	None	400 kHz	14-Lead TSSOP	RU-14	
AD5625BRUZ-REEL7 ¹	-40°C to +105°C	±1 LSB INL	None	400 kHz	14-Lead TSSOP	RU-14	
AD5625RBCPZ-R2 ¹	-40°C to +105°C	±1 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	CP-10-9	D8S
AD5625RBCPZ-REEL7 ¹	-40°C to +105°C	±1 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	CP-10-9	D8S
AD5625RBRUZ-1 ¹	-40°C to +105°C	±1 LSB INL	2.5 V	400 kHz	14-Lead TSSOP	RU-14	
AD5625RBRUZ-1REEL7 ¹	-40°C to +105°C	±1 LSB INL	2.5 V	400 kHz	14-Lead TSSOP	RU-14	
AD5625RBRUZ-2 ¹	-40°C to +105°C	±1 LSB INL	2.5 V	3.4 MHz	14-Lead TSSOP	RU-14	
AD5625RBRUZ-2REEL7 ¹	-40°C to +105°C	±1 LSB INL	2.5 V	3.4 MHz	14-Lead TSSOP	RU-14	
AD5645RBCPZ-R2 ¹	-40°C to +105°C	±4 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	RU-14	D89
AD5645RBCPZ-REEL7 ¹	-40°C to +105°C	±4 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	RU-14	D89
AD5645RBRUZ ¹	-40°C to +105°C	±4 LSB INL	2.5 V	400 kHz	14-Lead TSSOP	RU-14	
AD5645RBRUZ-REEL7 ¹	-40°C to +105°C	±4 LSB INL	2.5 V	400 kHz	14-Lead TSSOP	RU-14	
AD5665BCPZ-R2 ¹	-40°C to +105°C	±16 LSB INL	None	400 kHz	10-Lead LFCSP_WD	CP-10-9	D6U
AD5665BCPZ-REEL7 ¹	-40°C to +105°C	±16 LSB INL	None	400 kHz	10-Lead LFCSP_WD	CP-10-9	D6U
AD5665BRUZ ¹	-40°C to +105°C	±16 LSB INL	None	400 kHz	14-Lead TSSOP	RU-14	
AD5665BRUZ-REEL7 ¹	-40°C to +105°C	±16 LSB INL	None	400 kHz	14-Lead TSSOP	RU-14	
AD5665RBCPZ-R2 ¹	-40°C to +105°C	±16 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	CP-10-9	DA2
AD5665RBCPZ-REEL7 ¹	-40°C to +105°C	±16 LSB INL	1.25 V	400 kHz	10-Lead LFCSP_WD	CP-10-9	DA2
AD5665RBRUZ-1 ¹	-40°C to +105°C	±16 LSB INL	2.5 V	400 kHz	14-Lead TSSOP	RU-14	
AD5665RBRUZ-1REEL7 ¹	-40°C to +105°C	±16 LSB INL	2.5 V	400 kHz	14-Lead TSSOP	RU-14	
AD5665RBRUZ-2 ¹	-40°C to +105°C	±16 LSB INL	2.5 V	3.4 MHz	14-Lead TSSOP	RU-14	
AD5665RBRUZ-2REEL7 ¹	-40°C to +105°C	±16 LSB INL	2.5 V	3.4 MHz	14-Lead TSSOP	RU-14	
EVAL-AD5665REBZ1 ¹					Evaluation Board		
EVAL-AD5665REBZ2 ¹					Evaluation Board		

¹ Z = RoHS Compliant Part.

AD5625R/AD5645R/AD5665R, AD5625/AD5665

NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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